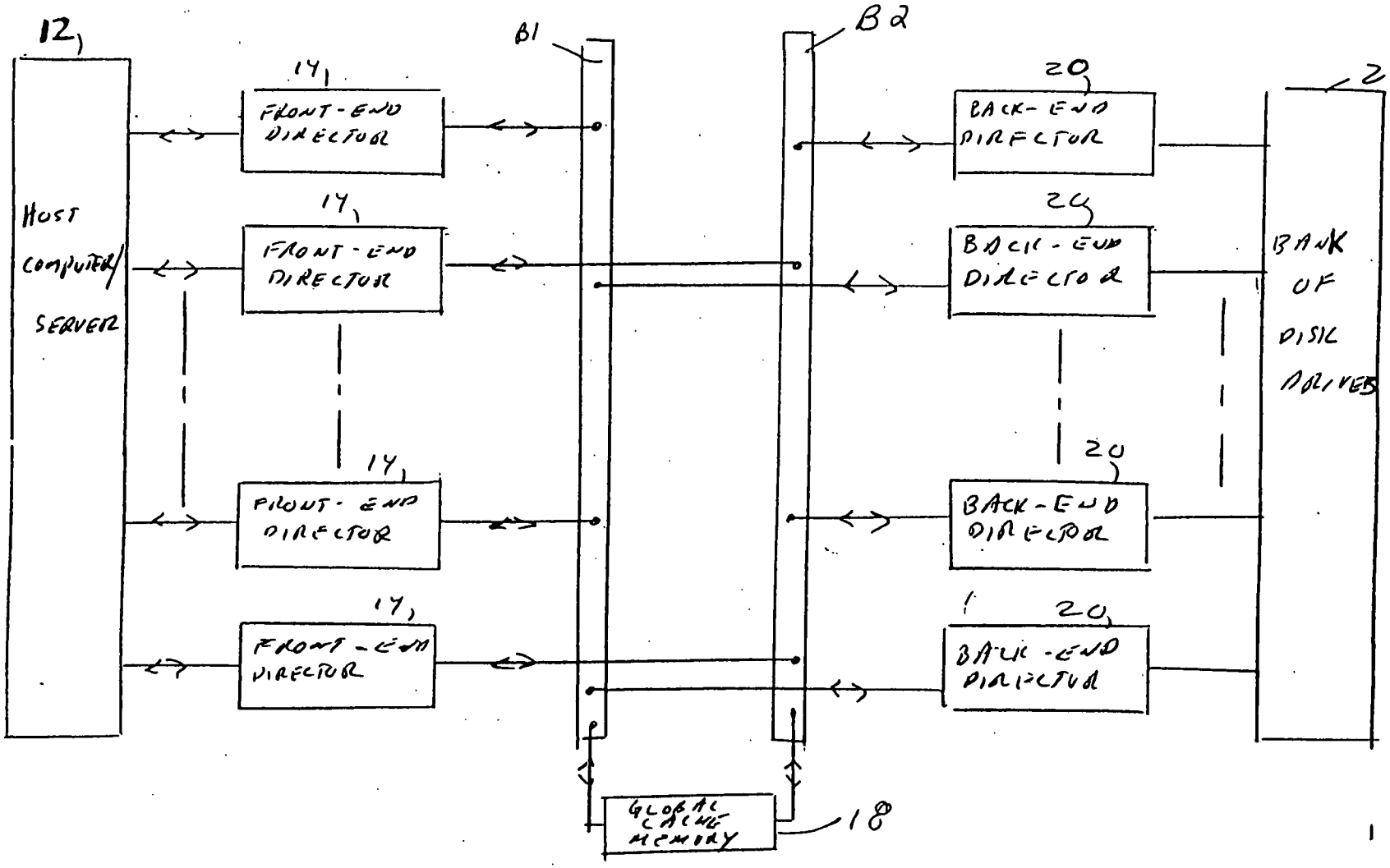
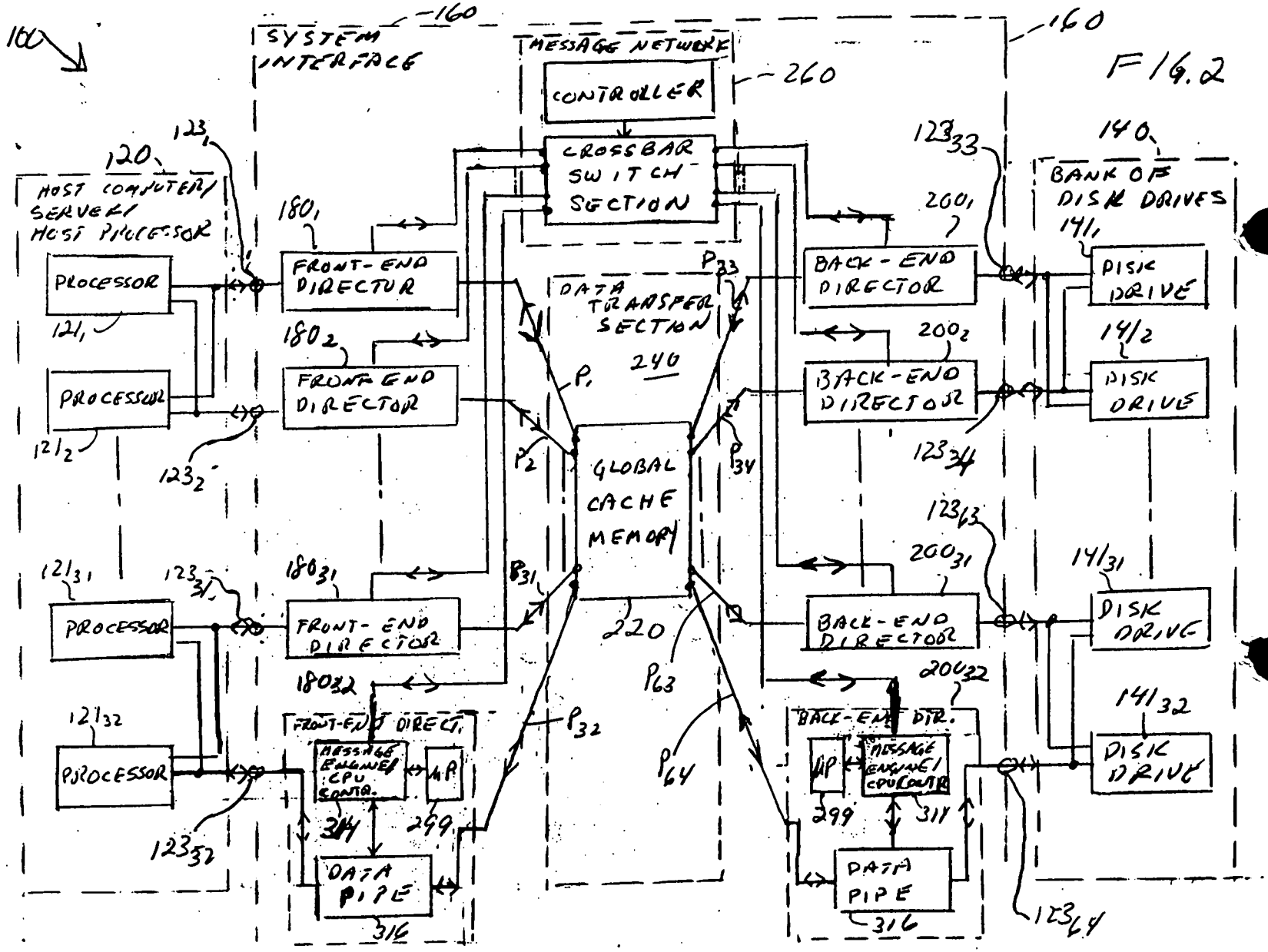
FIG. 1
PRIOR ART





F16.2

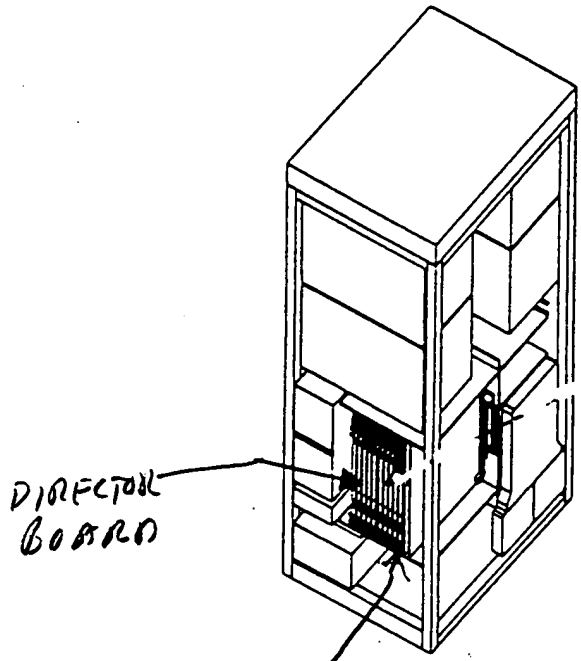
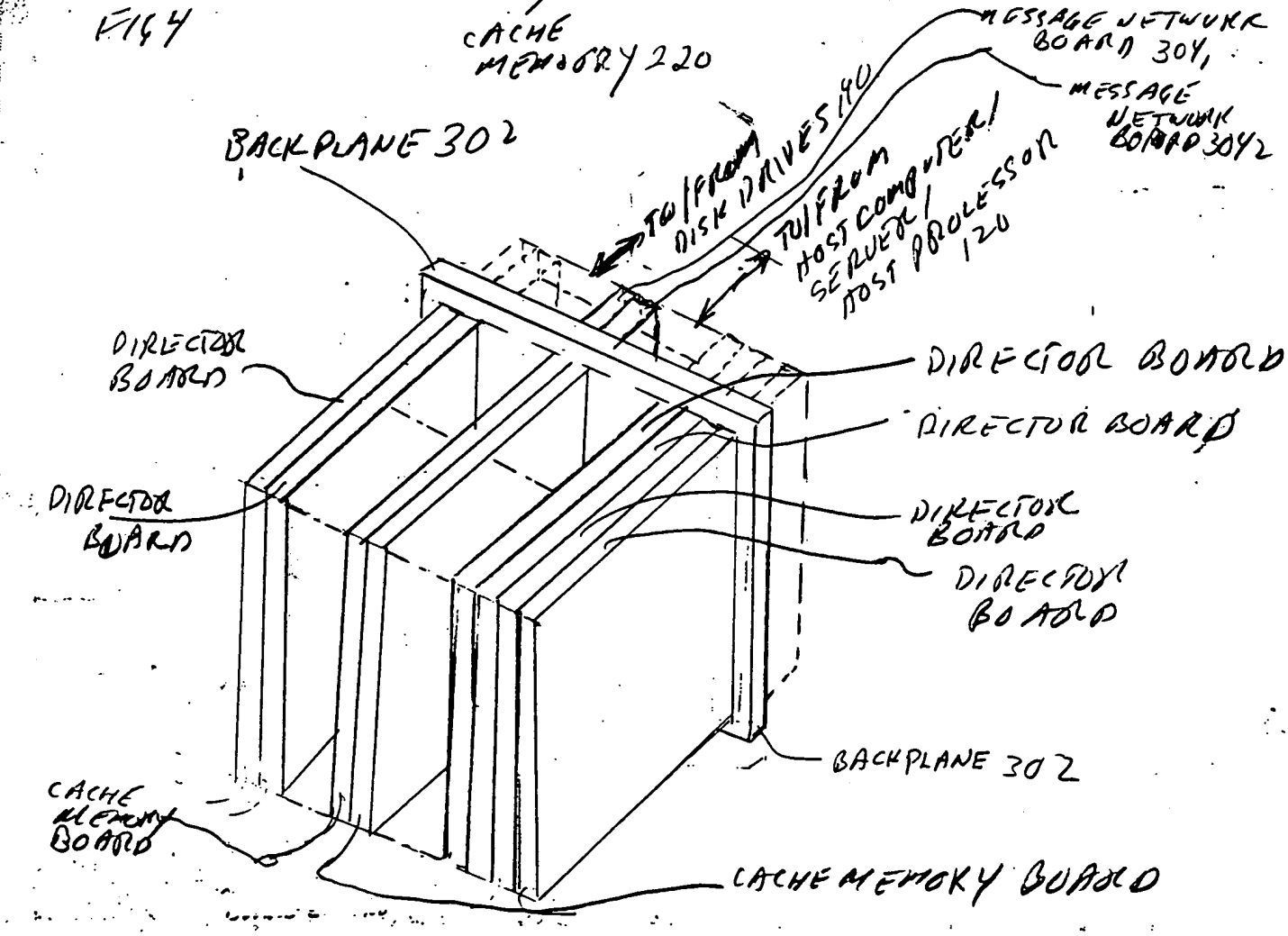
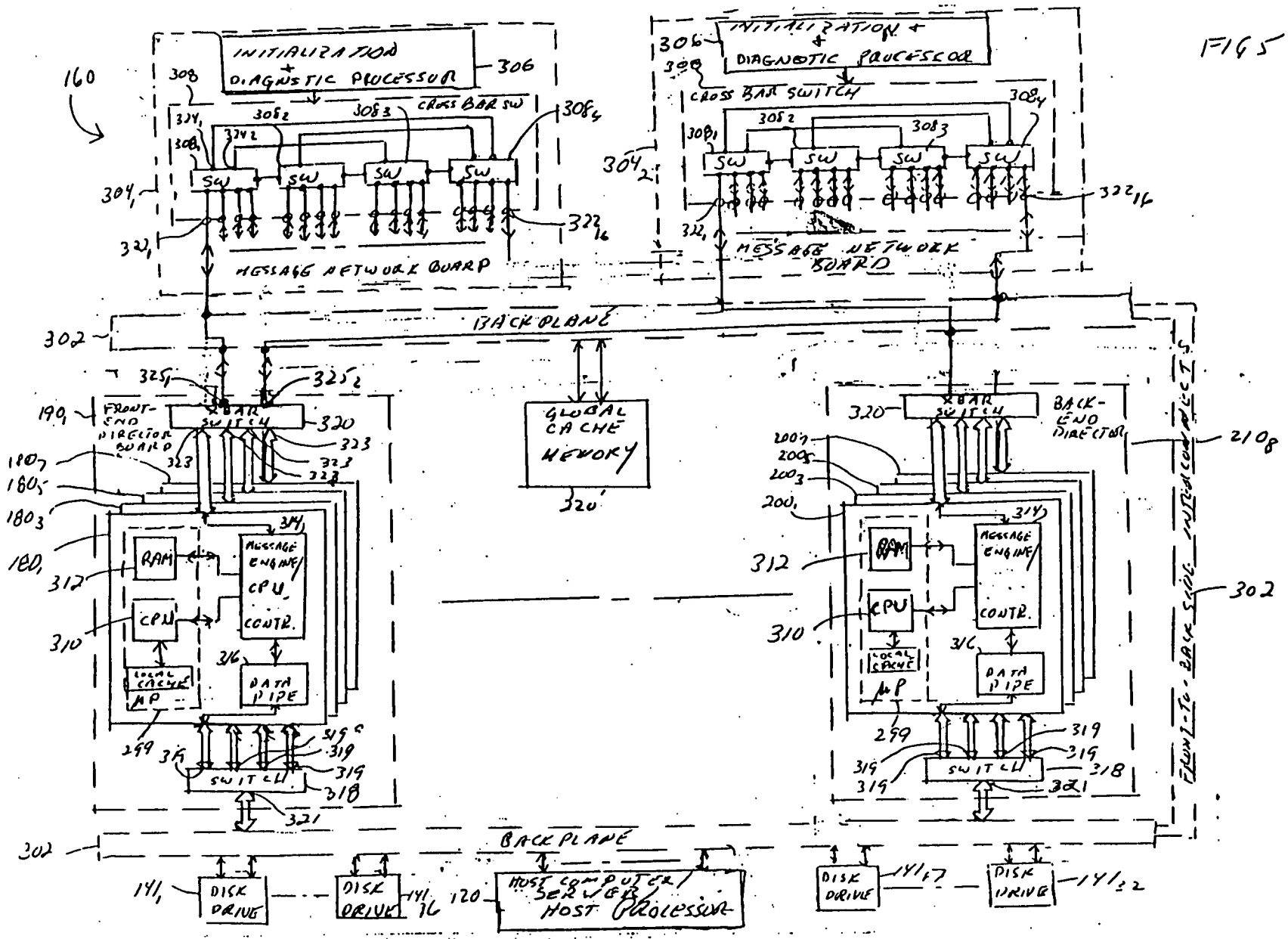

DIRECTOR BOARD
CACHE MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304 2
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD


160
INITIALIZATION + DIAGNOSTIC PROCESSOR
306
CROSS BAR SW
CROSS BAR SWITCH
MESSAGE NETWORK BOARD
BACKPLANE
GLOBAL CACHE MEMORY
320'
FRONT-END DIRECTOR BOARD
BACK-END DIRECTOR
XBAR SWITCH
320
RAM
MESSAGE ENGINE/ CPU CONTR.
CPU
LOCAL CACHE
μP
DATA PIPE
SWITCH
318
DISK DRIVE
HOST COMPUTER/ SERVER/ HOST PROCESSOR
120
FIG 5 - BACK SIDE INTERCONNECT

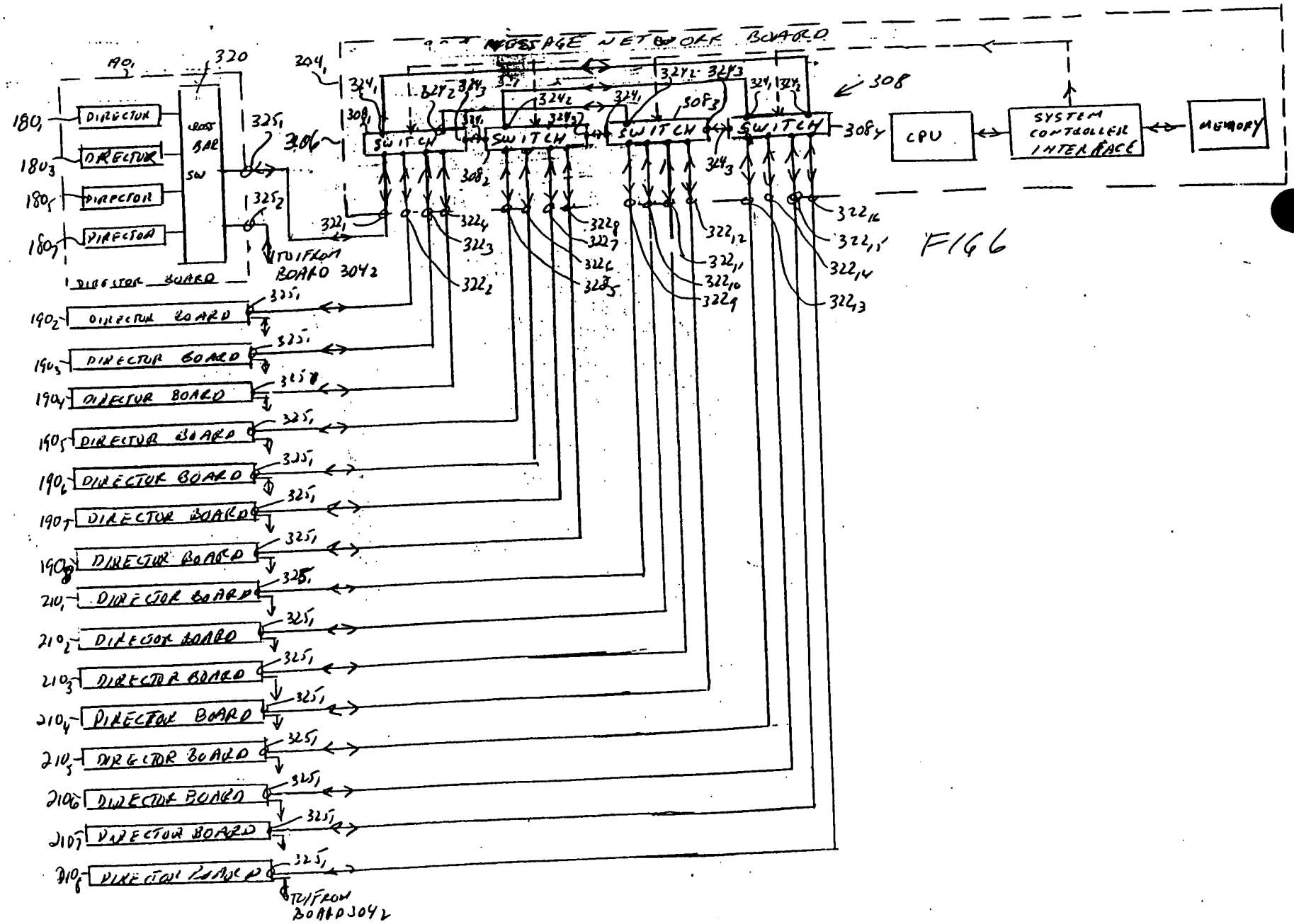
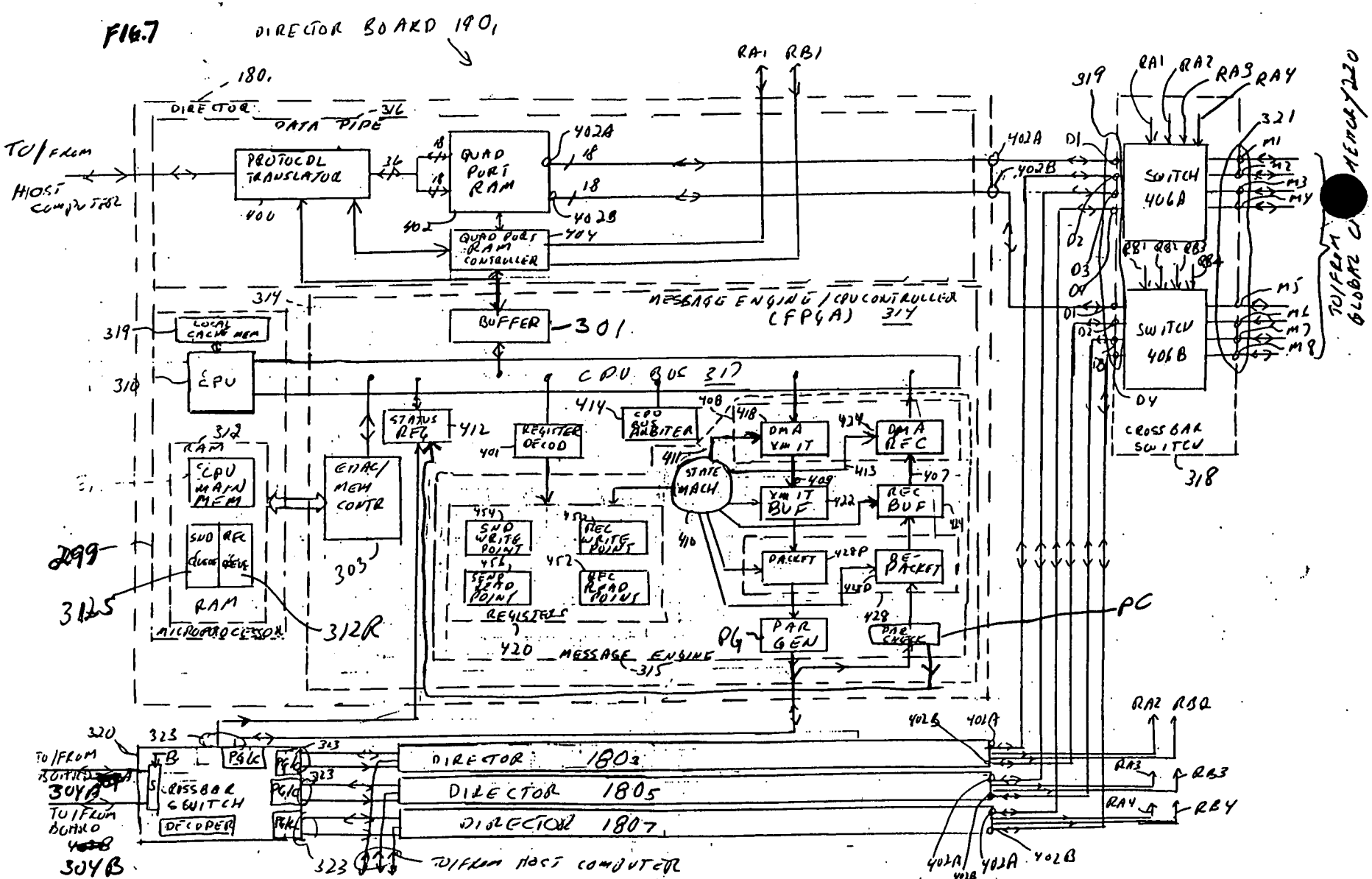
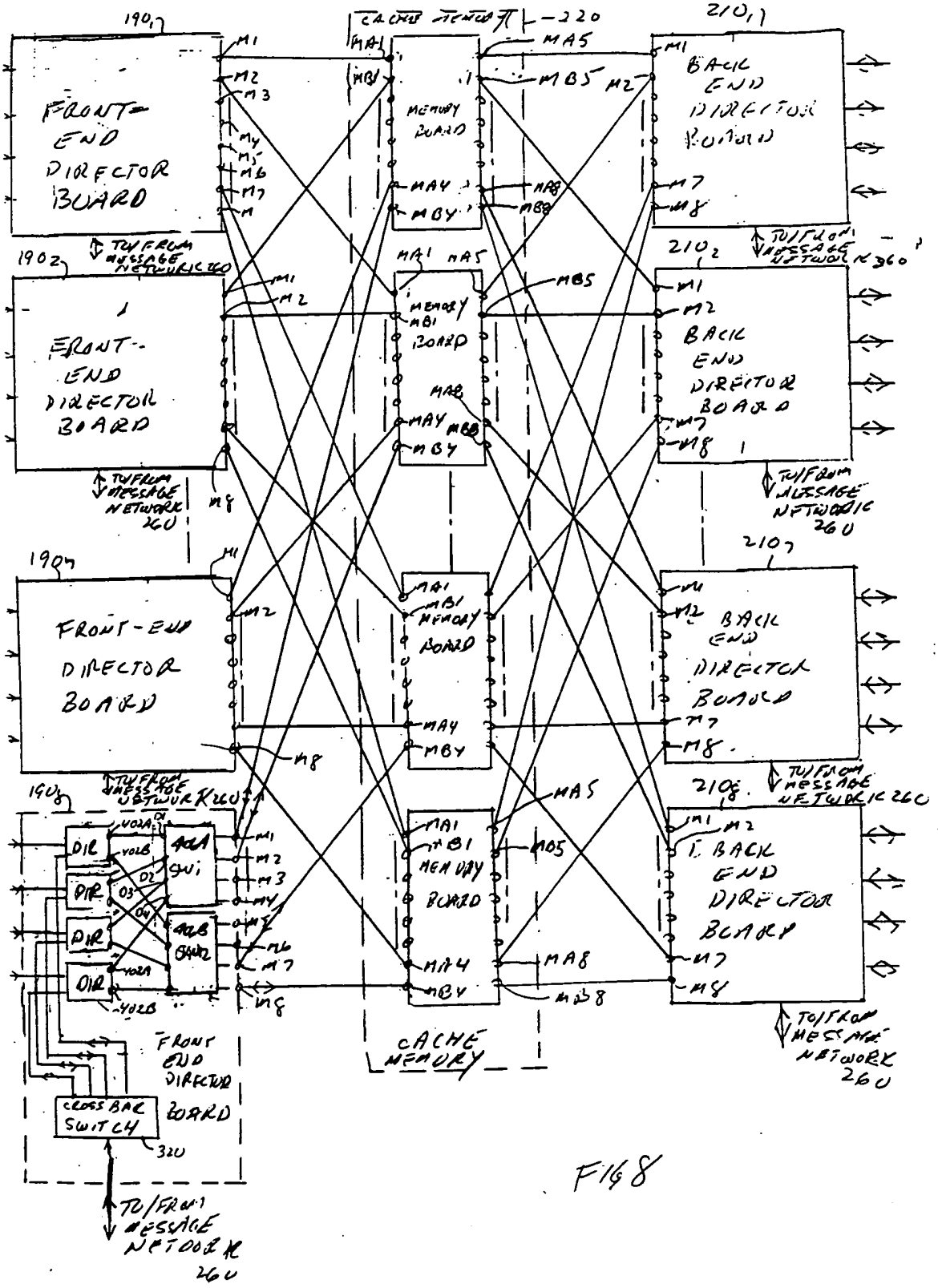


FIG 6

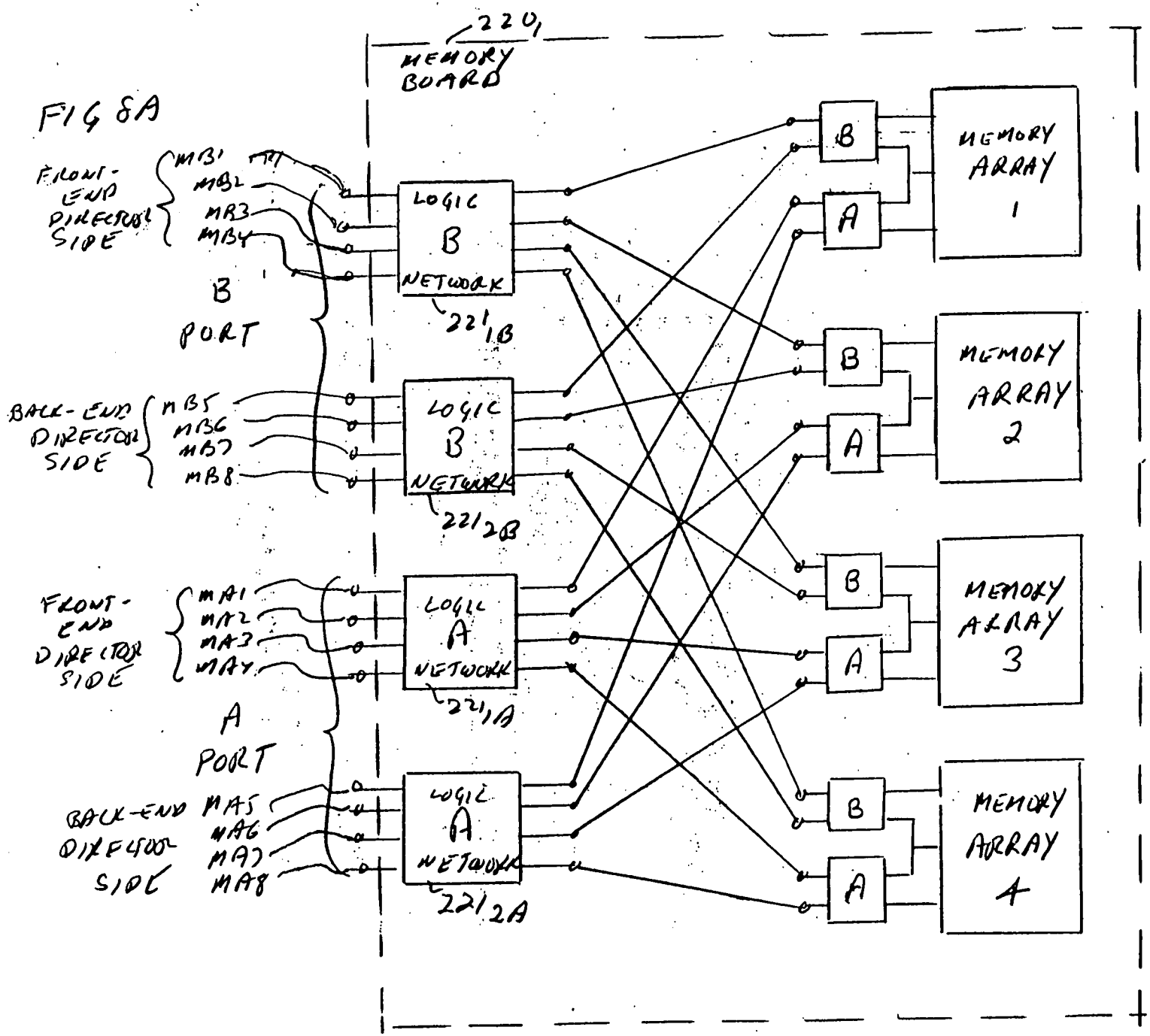
FIG. 7




190,
FRONT-END DIRECTOR BOARD
CACHE MEMORY
220
210,
BACK END DIRECTOR BOARD
MEMORY BOARD
TO/FROM MESSAGE NETWORK 260
190 2
210 2
190 7
210 7
190 8
210 8
DIR
ADA
ADB
CROSS BAR SWITCH
320
FRONT END DIRECTOR BOARD
TO/FROM MESSAGE NETWORK 260

F16 8

FIG 8A



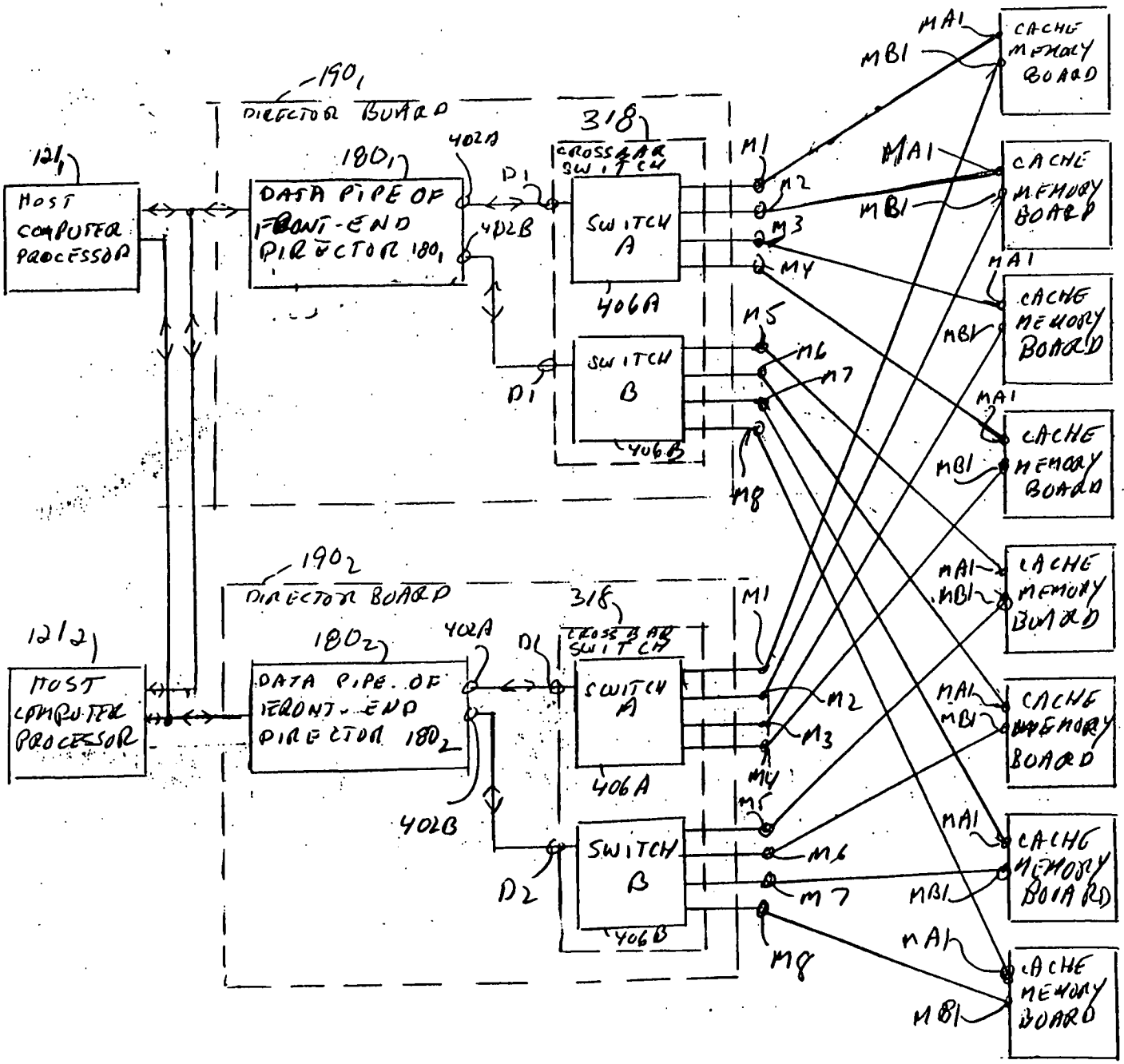

HOST COMPUTER PROCESSOR
121
DIRECTOR BOARD
190
DATA PIPE OF FRONT-END DIRECTOR
180
402A
402B
D1
D2
CROSS BAR SWITCH
318
SWITCH A
406A
SWITCH B
406B
M1
M2
M3
M4
M5
M6
M7
M8
MA1
MB1
CACHE MEMORY BOARD

FIG 8B

FIG. 8C

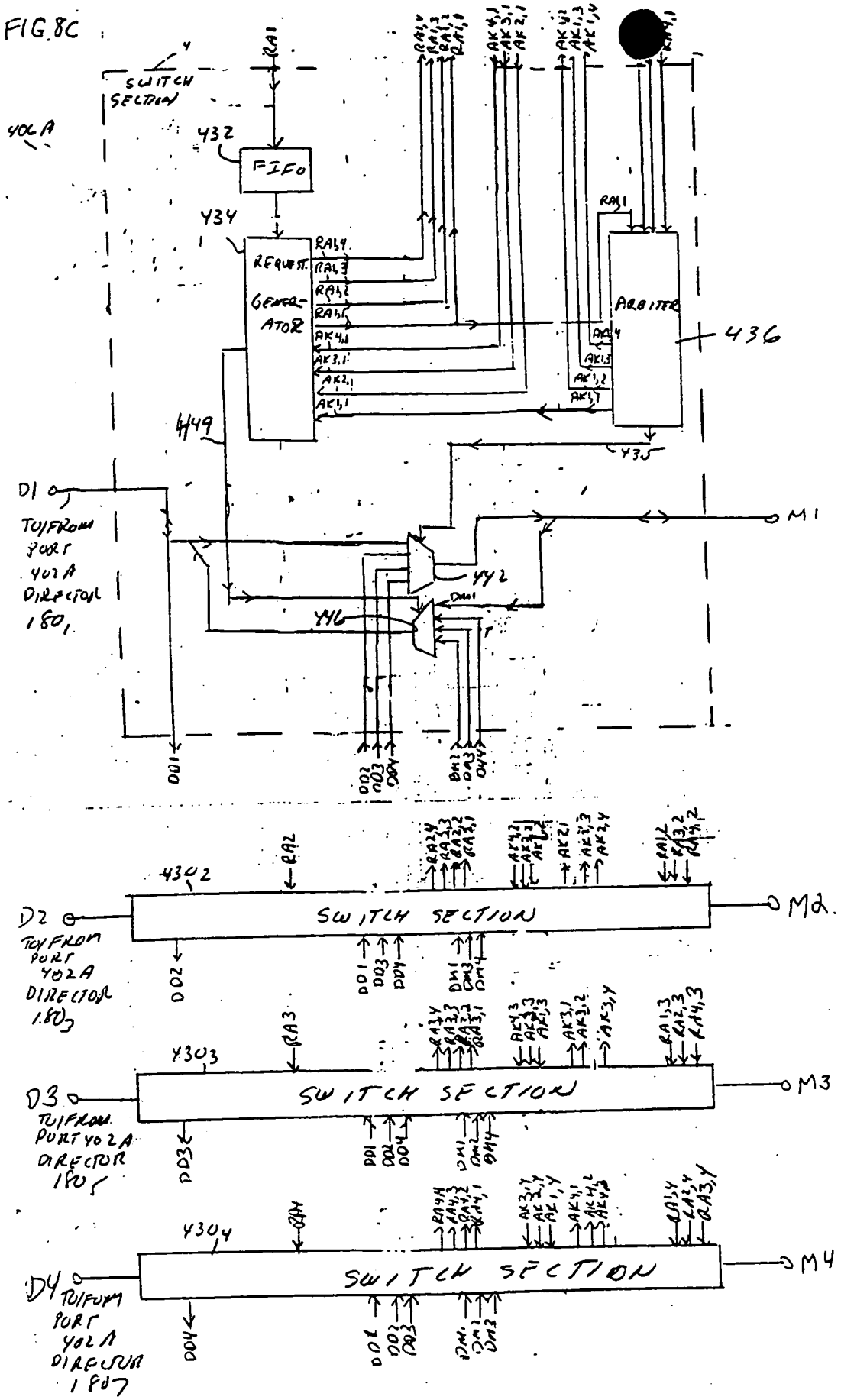

SWITCH SECTION
402A
432
FIFO
434
REQUEST GENERATOR
449
ARBITER
436
435
D1
TO/FROM PORT 402A DIRECTOR 180
M1
442
446
D2
TO/FROM PORT 402A DIRECTOR 180
M2
SWITCH SECTION
443
D3
TO/FROM PORT 402A DIRECTOR 180
M3
SWITCH SECTION
444
D4
TO/FROM PORT 402A DIRECTOR 180
M4
SWITCH SECTION

FIG 9

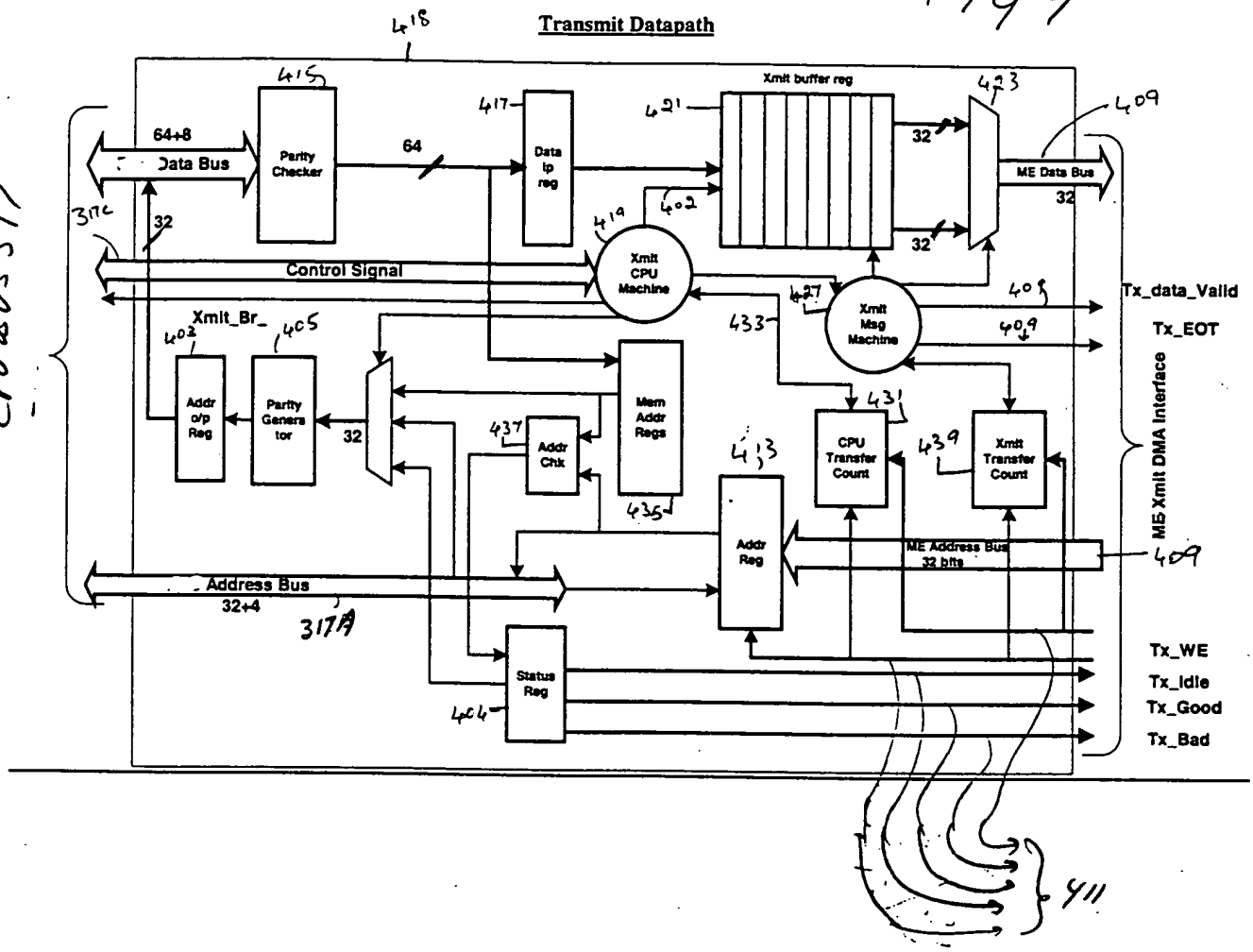
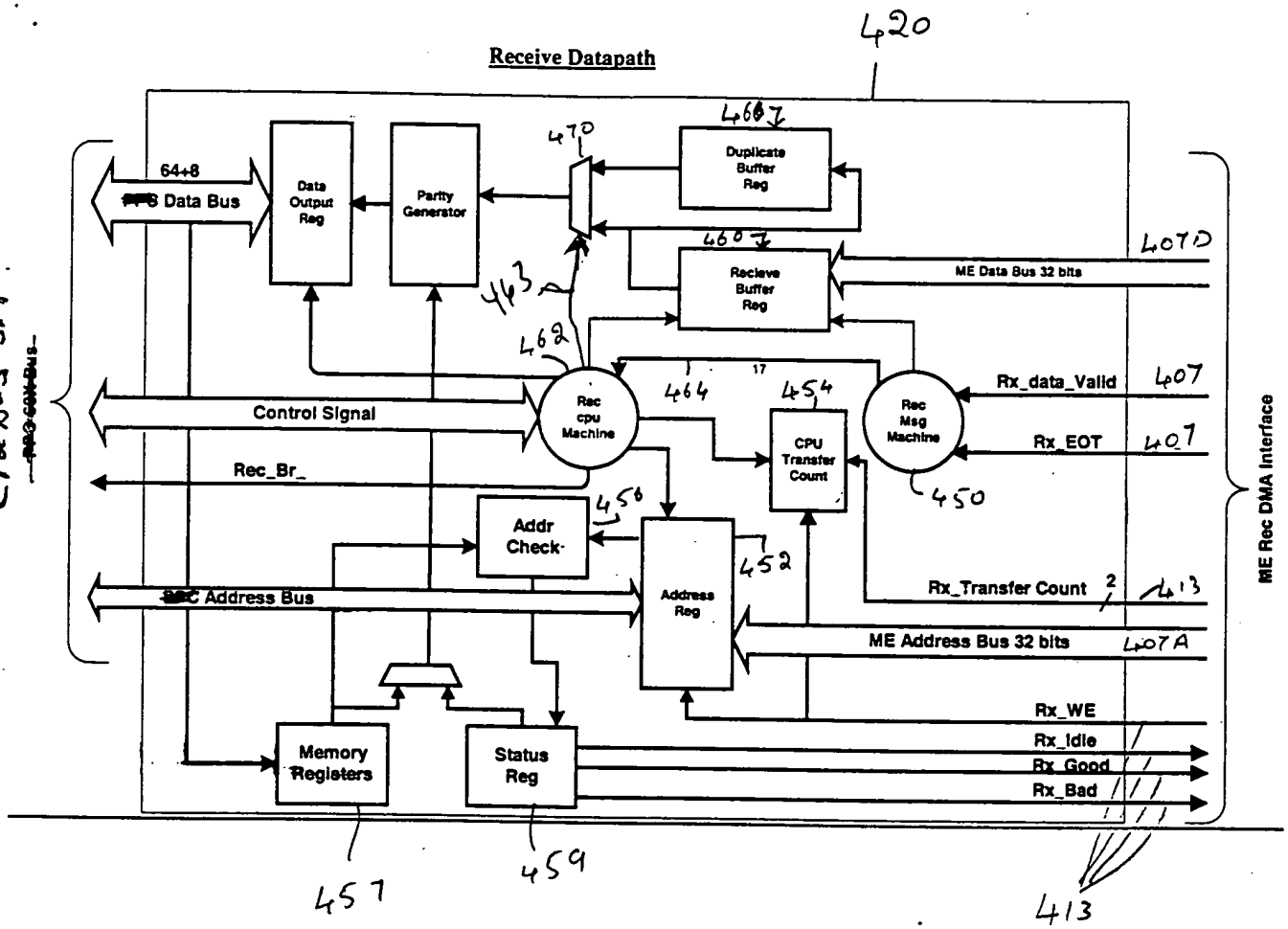

Transmit Datapath
418
415
417
421
Xmit buffer reg
423
409
64+8
Data Bus
Parity Checker
64
Data Ip reg
32
ME Data Bus
32
317c
32
419
402
Xmit CPU Machine
Control Signal
427
Xmit Msg Machine
409
Tx_data_Valid
Tx_EOT
433
Xmit_Br_
402
405
Addr o/p Reg
Parity Generator
32
Mem Addr Regs
431
437
Addr Chk
CPU Transfer Count
439
Xmit Transfer Count
413
435
Addr Reg
ME Address Bus 32 bits
409
ME Xmit DMA Interface
Address Bus
32+4
317A
Status Reg
404
Tx_WE
Tx_Idle
Tx_Good
Tx_Bad
411
CPU BUS 317

FIG 10


Receive Datapath
420
64+8
Data Bus
Data Output Reg
Parity Generator
470
Duplicate Buffer Reg
460
Recieve Buffer Reg
ME Data Bus 32 bits
407D
463
462
464
454
Rec cpu Machine
Rec Msg Machine
Rx_data_Valid
407
Rx_EOT
407
Control Signal
Rec_Br_
CPU Transfer Count
450
456
Addr Check
452
Address Reg
Rx_Transfer Count
2
413
Address Bus
ME Address Bus 32 bits
407A
Rx_WE
Rx_Idle
Rx_Good
Rx_Bad
Memory Registers
Status Reg
457
459
413
CPU BUS 317
ME Rec DMA Interface

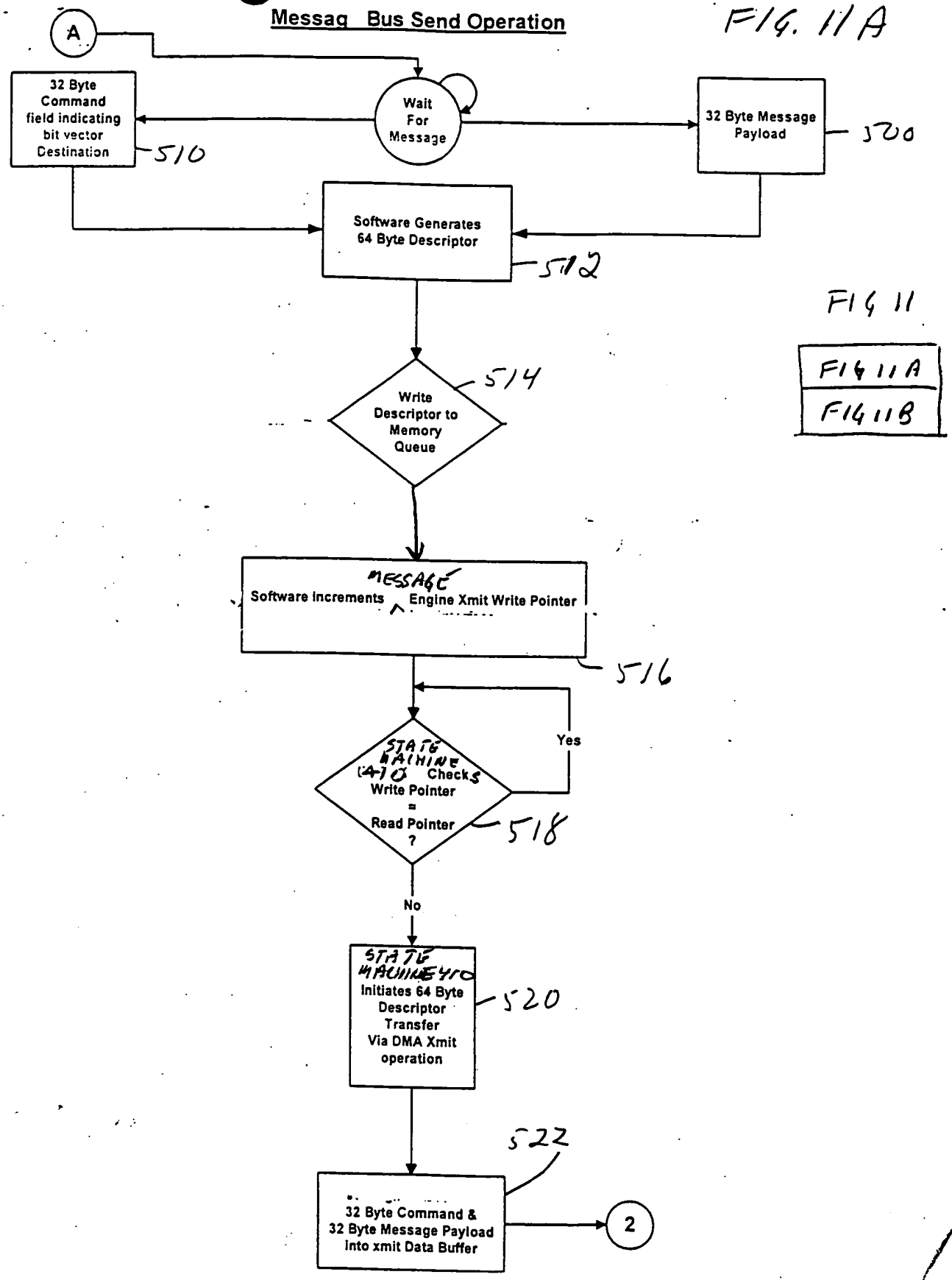


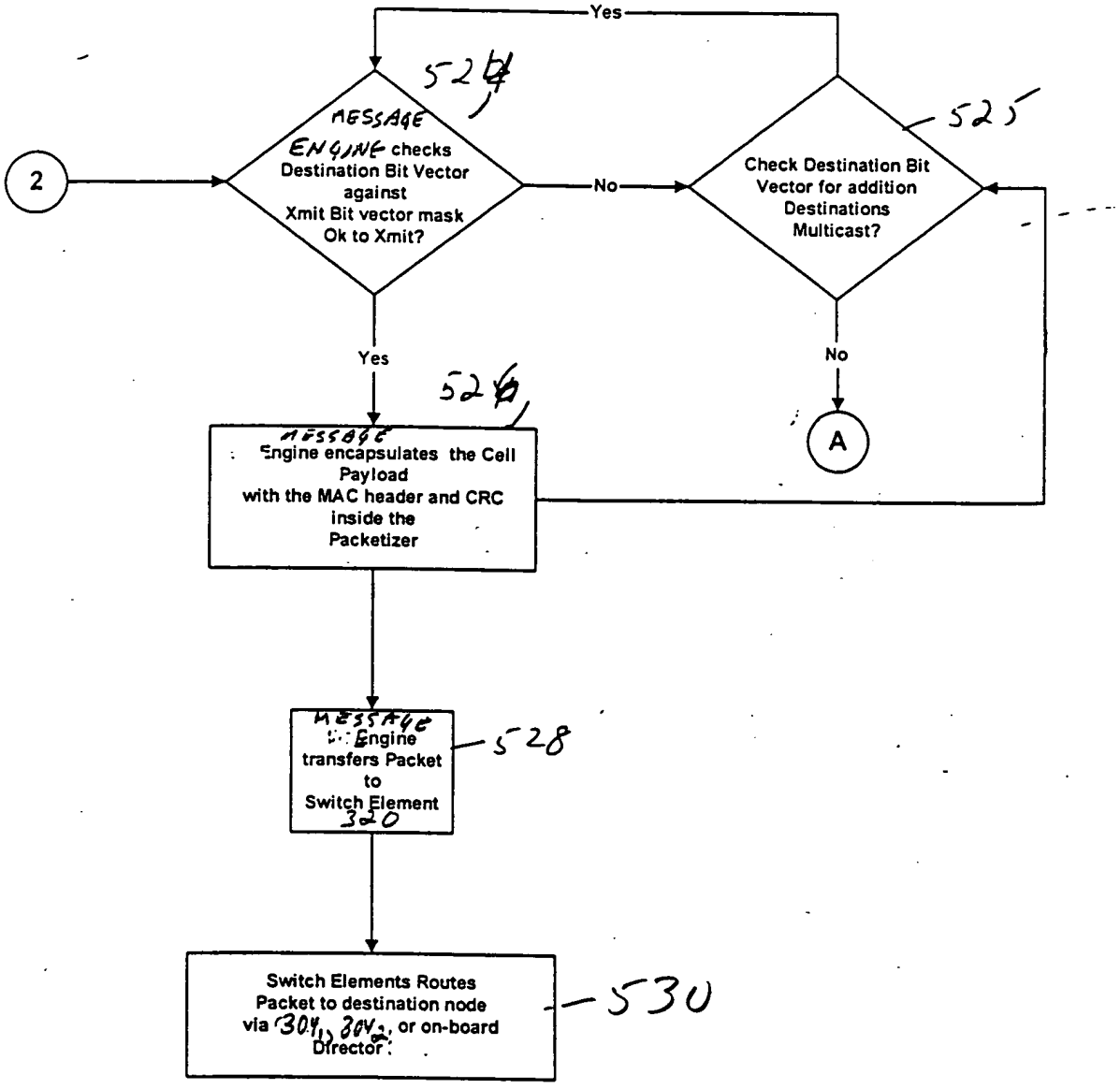
FIG. 11A

FIG 11

FIG 11A
FIG 11B

Message Bus Send Op ration Continued

FIG 11B



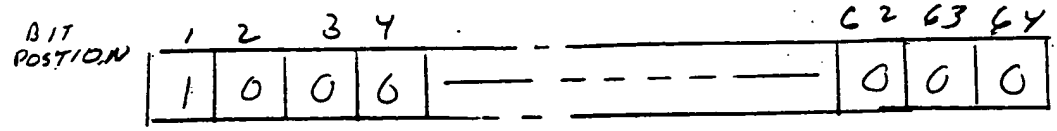


FIG 11C

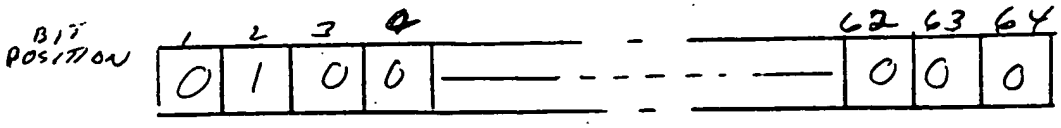


FIG 11D

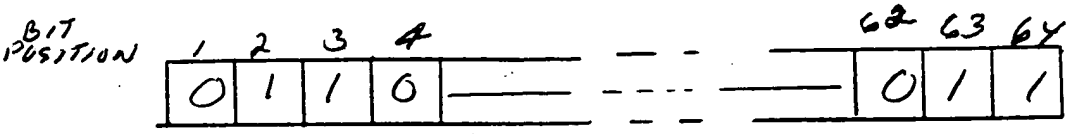


FIG 11E

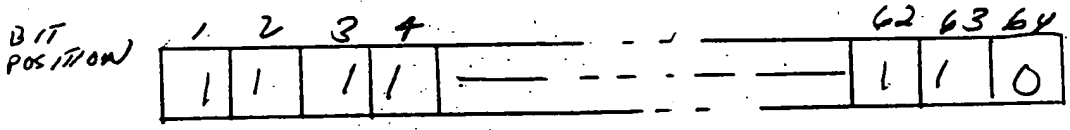


FIG 11F

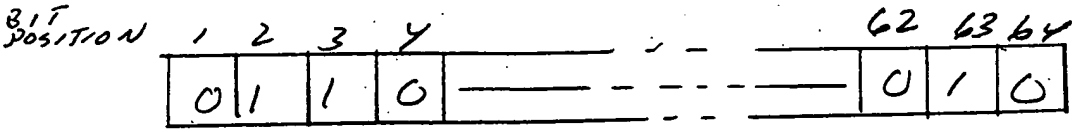


FIG 11G

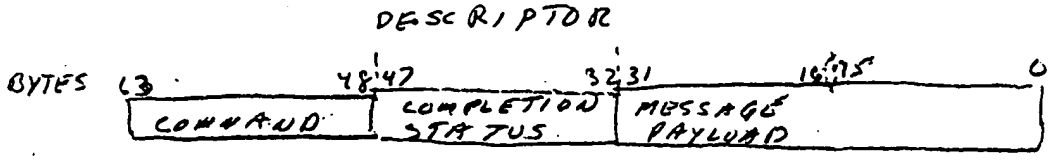


FIG 2A

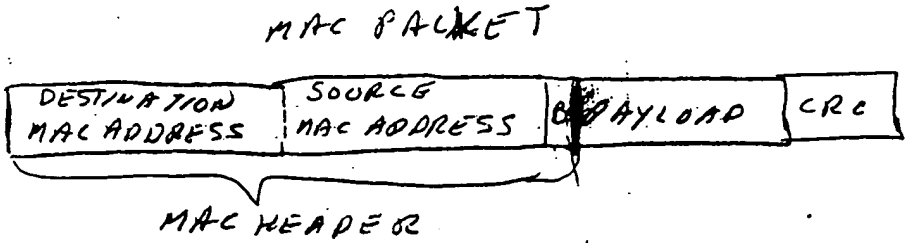


FIG 2B

M ssage Bus Receive Operation

FIG. 12A

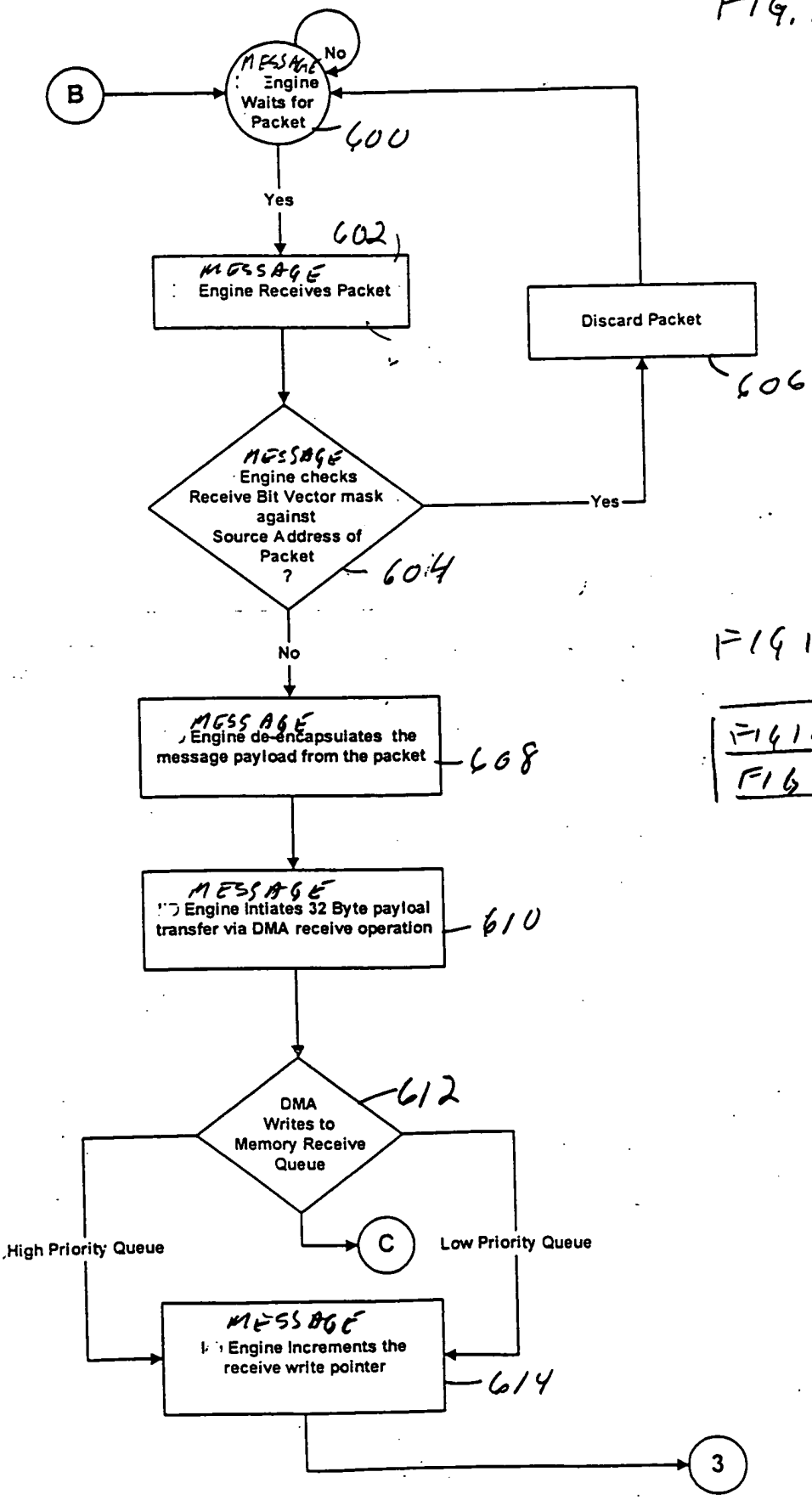


FIG 12

FIG 12A
FIG 12B

Message Bus Receive Operation Continued

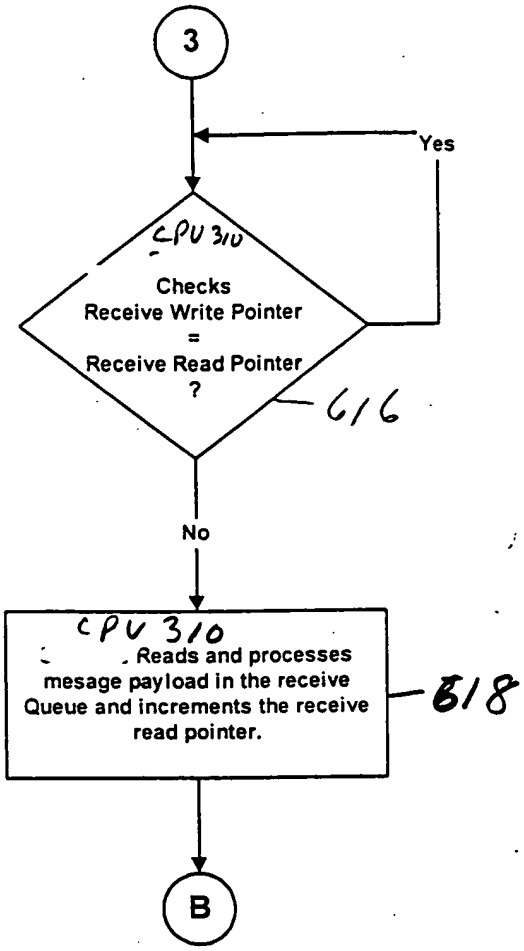


FIG 12B

Message Bus Acknowledgement Op ration

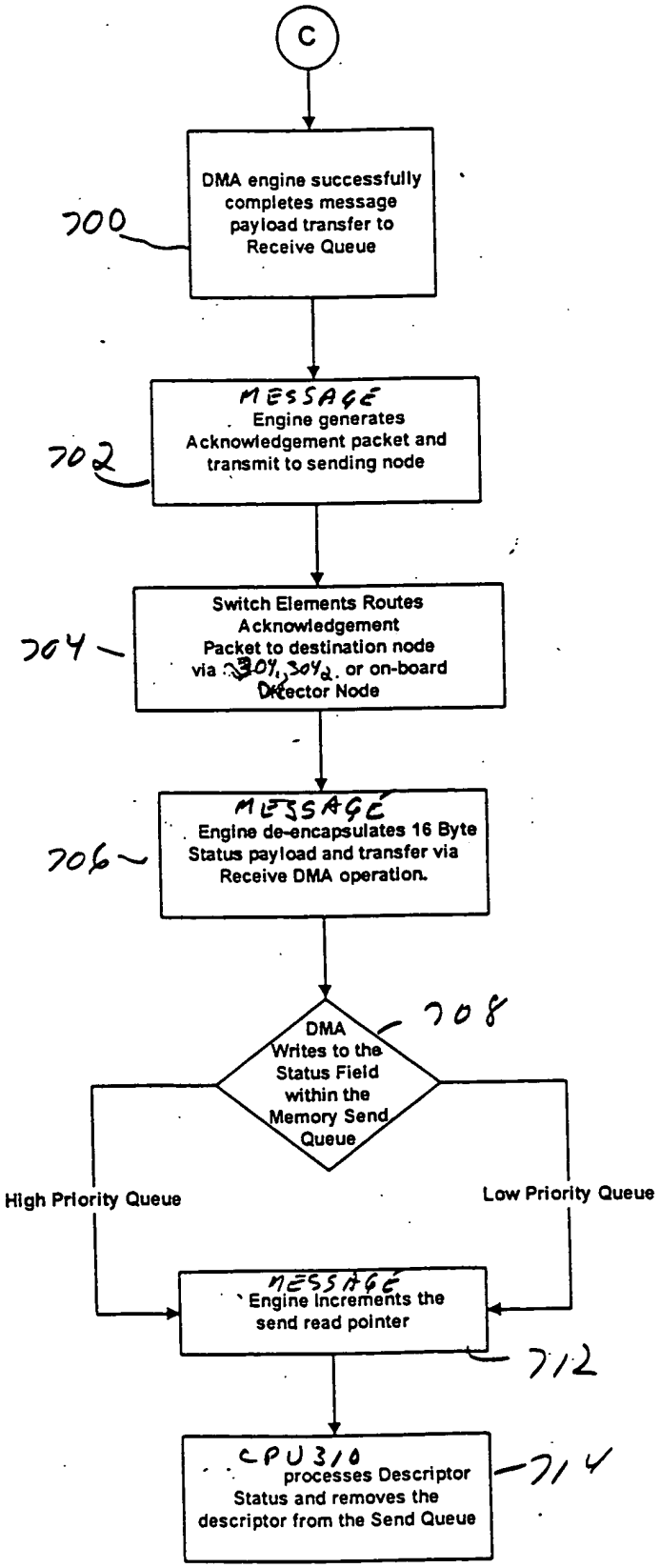


Fig. 13

FIG 14A

Xmit CPU flow

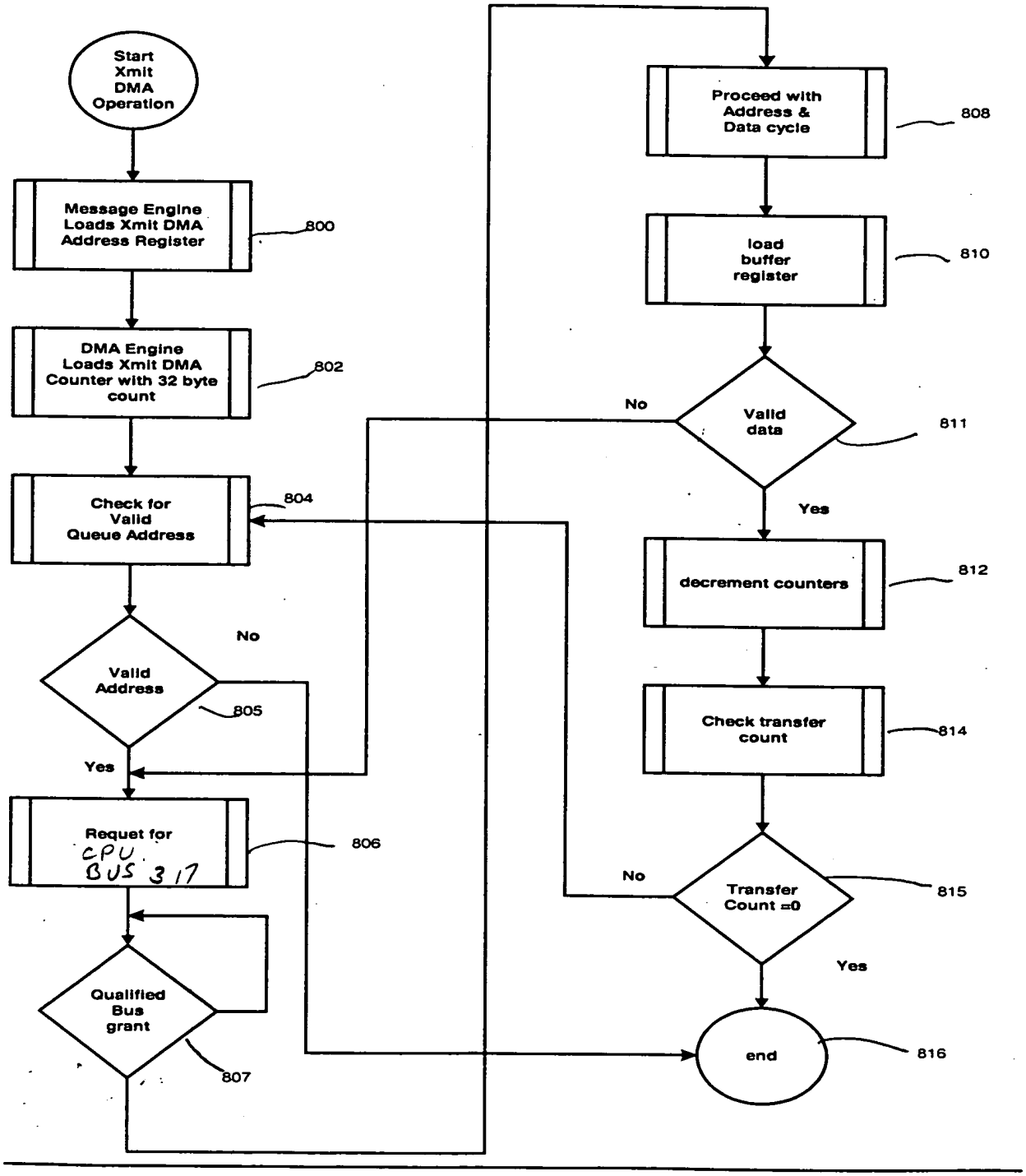


FIG 8B

Xmit Msg flow

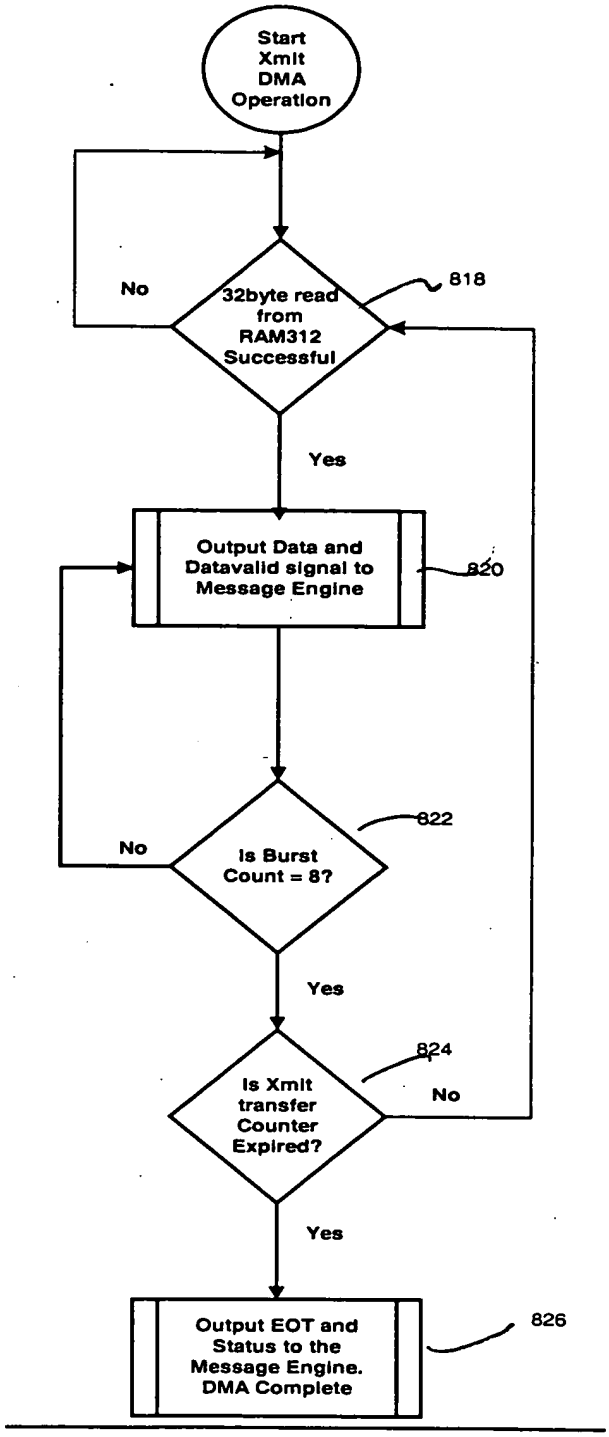


FIG 15A

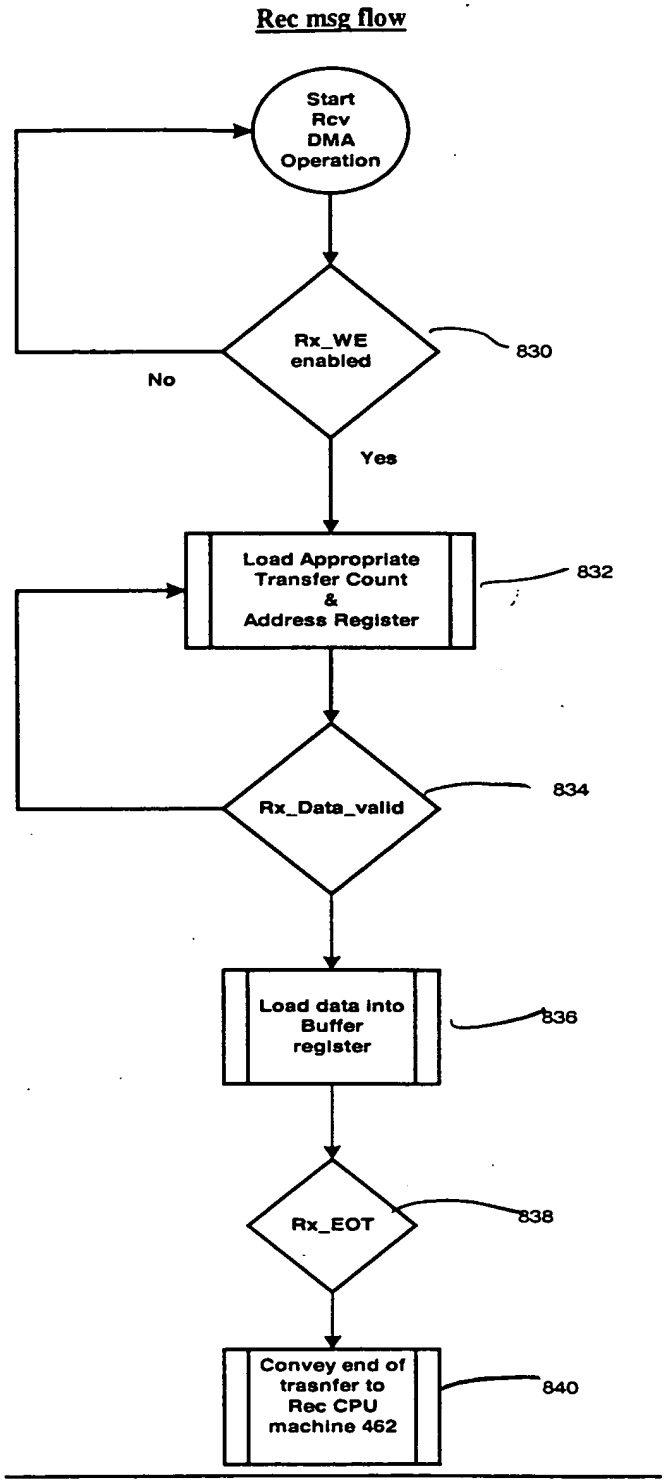

Rec msg flow
Start Rcv DMA Operation
Rx_WE enabled
830
No
Yes
Load Appropriate Transfer Count & Address Register
832
Rx_Data_valid
834
Load data into Buffer register
836
Rx_EOT
838
Convey end of trasnfer to Rec CPU machine 462
840

FIG 15B

Rec cpu flow